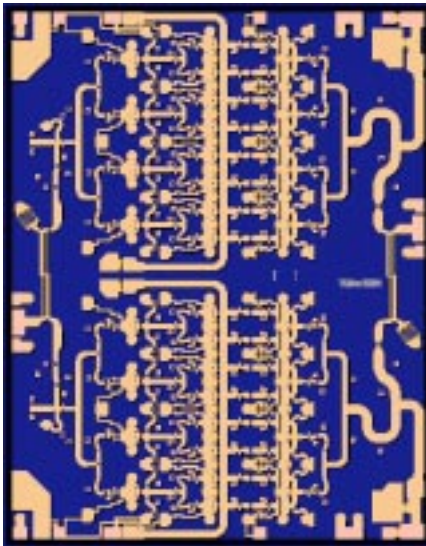


2W Q-Band High Power Amplifier

TGA4046-EPU



Key Features

- Typical Frequency Range: 41 - 46 GHz
- Typical 33dBm Psat, 32dBm P1dB
- 17 dB Nominal Gain
- 16 dB Nominal Return Loss
- Bias: 6 V, 2 A
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 3.45 x 4.39 x 0.10 mm (0.136 x 0.173 x 0.004 in)

Primary Applications

- Sat - Com

Product Description

The TriQuint TGA4046-EPU is a compact High Power Amplifier MMIC for Q-band applications. The part is designed using TriQuint's 0.15um gate power pHEMT process.

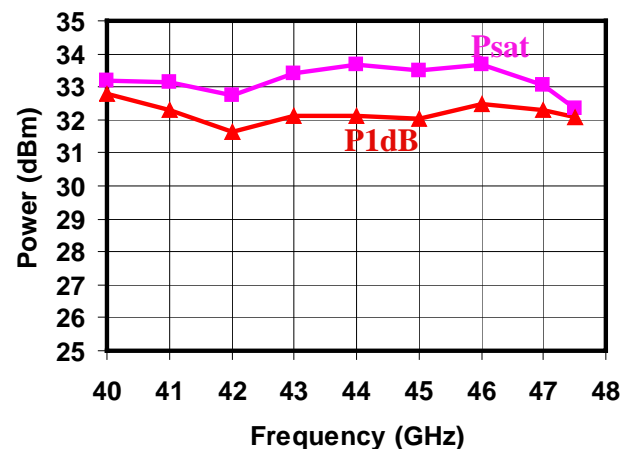
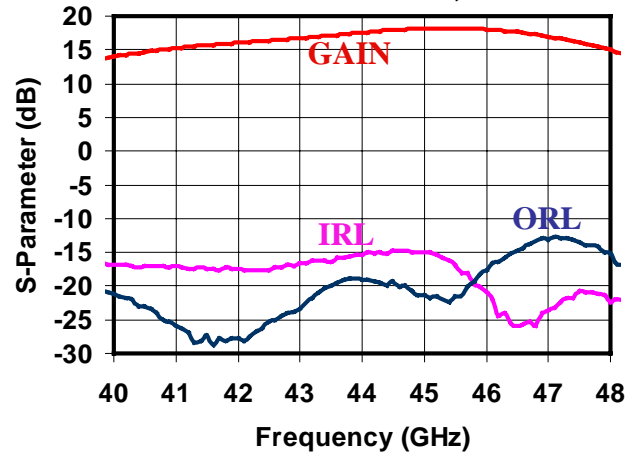
The TGA4046-EPU nominally provides 33dBm of Saturated Output Power, and 32dBm Output Power at 1dB gain compression from 41 - 46GHz. The MMIC also provides 17dB Gain and 16dB Return Loss.

The part is ideally suited for markets such as Satellite Communications both commercial and military.

The TGA4046-EPU is 100% DC and RF tested on-wafer to ensure performance compliance.

Measured Fixtured Data

Bias Conditions: Vd = 6 V, Id = 2 A



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V _d	Drain Voltage	7 V	<u>2/</u>
V _g	Gate Voltage Range	-2 TO 0 V	
I _d	Drain Current	3 A	<u>2/ 3/</u>
I _g	Gate Current	112 mA	<u>3/</u>
P _{IN}	Input Continuous Wave Power	29 dBm	
P _D	Power Dissipation	16 W	<u>2/ 4/</u>
T _{CH}	Operating Channel Temperature	150 °C	<u>5/ 6/</u>
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 3/ Total current for the entire MMIC.
- 4/ When operated at this bias condition with a base plate temperature of 70°C, the median life is 1E+6 hrs.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 6/ These ratings apply to each individual FET.

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TABLE III
ELECTRICAL CHARACTERISTICS

(Ta = 25 °C Nominal)

PARAMETER	TYPICAL	UNITS
Frequency Range	41 - 46	GHz
Drain Voltage, Vd	6.0	V
Drain Current, Id	2	A
Gate Voltage, Vg	-0.6	V
Small Signal Gain, S21	17	dB
Input Return Loss, S11	18	dB
Output Return Loss, S22	20	dB
Output Power @ 1dB Gain Compression, P1dB	32	dBm
Saturated Power, Psat	33	dBm

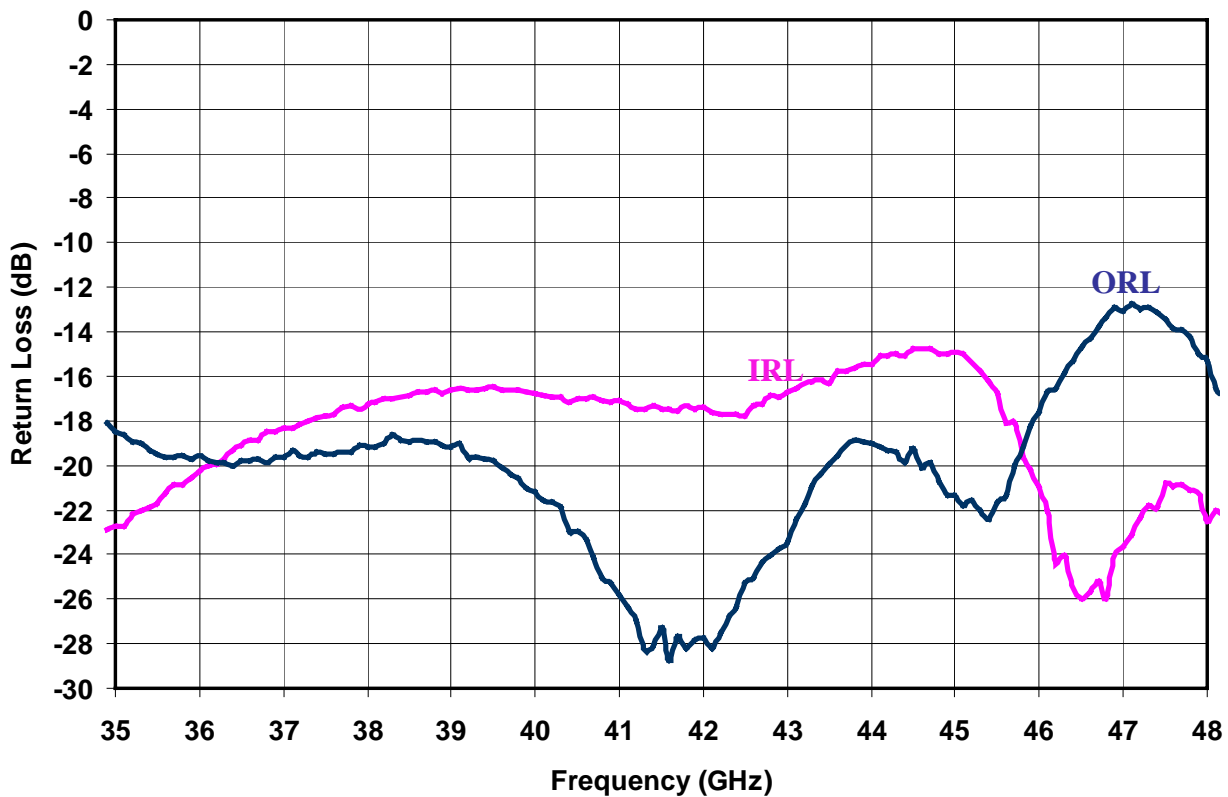
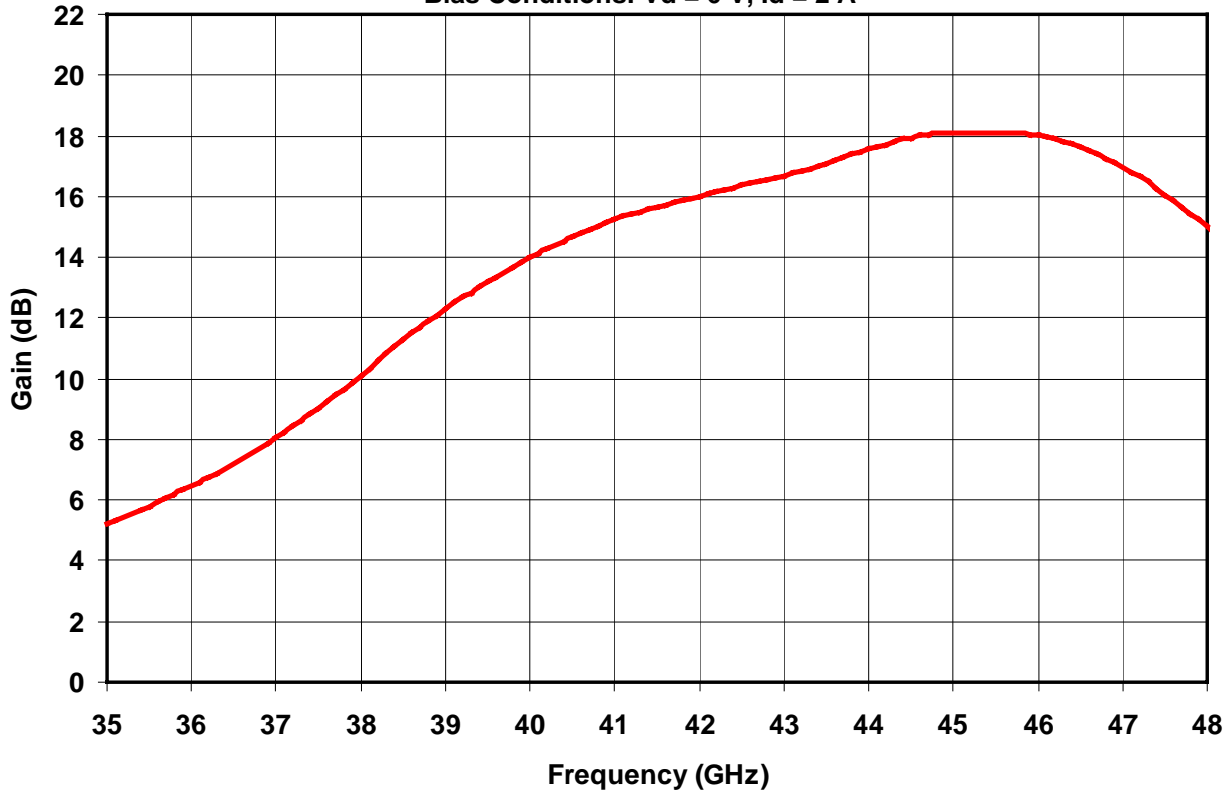
TABLE IV
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS	T _{CH} (°C)	R _{θJC} (°C/W)	T _M (HRS)
R _{θJC} Thermal Resistance (channel to Case)	Vd = 6 V Id = 2 A Pdiss = 12 W	129	4.9	6.4E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

Preliminary Measured Data

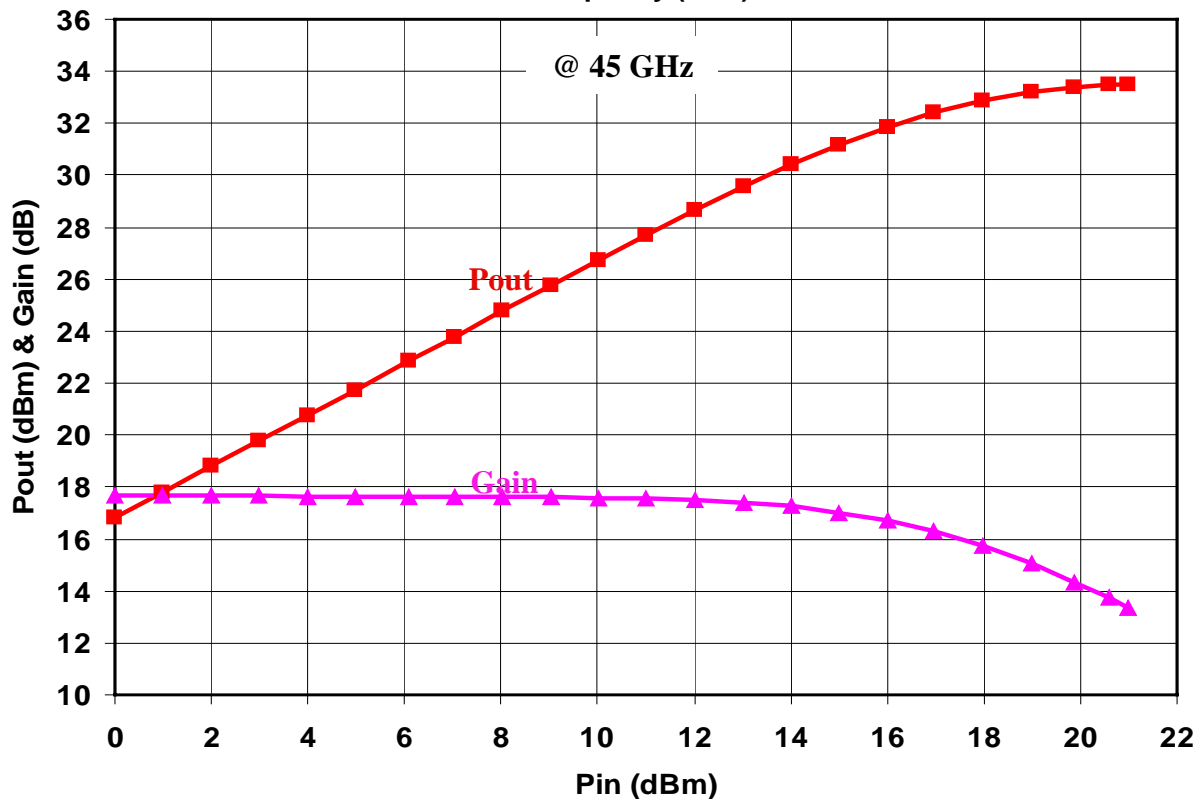
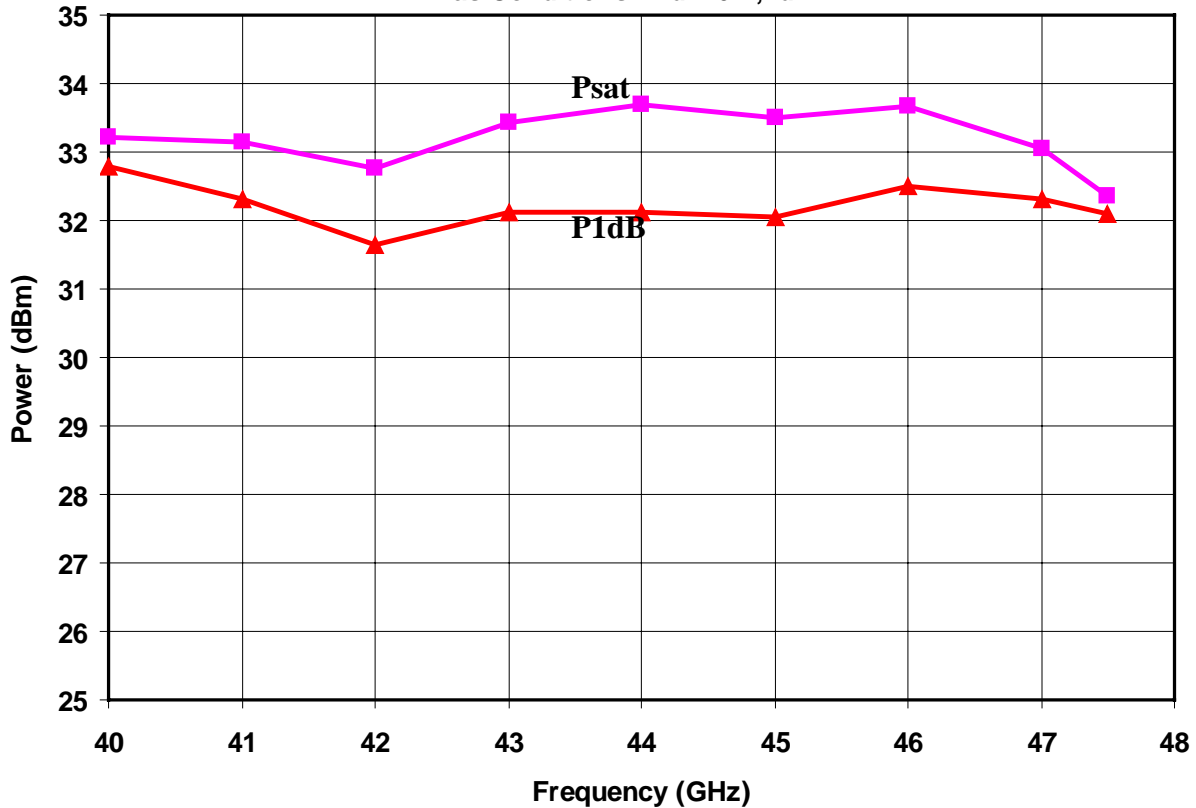
Bias Conditions: $V_d = 6\text{ V}$, $I_d = 2\text{ A}$



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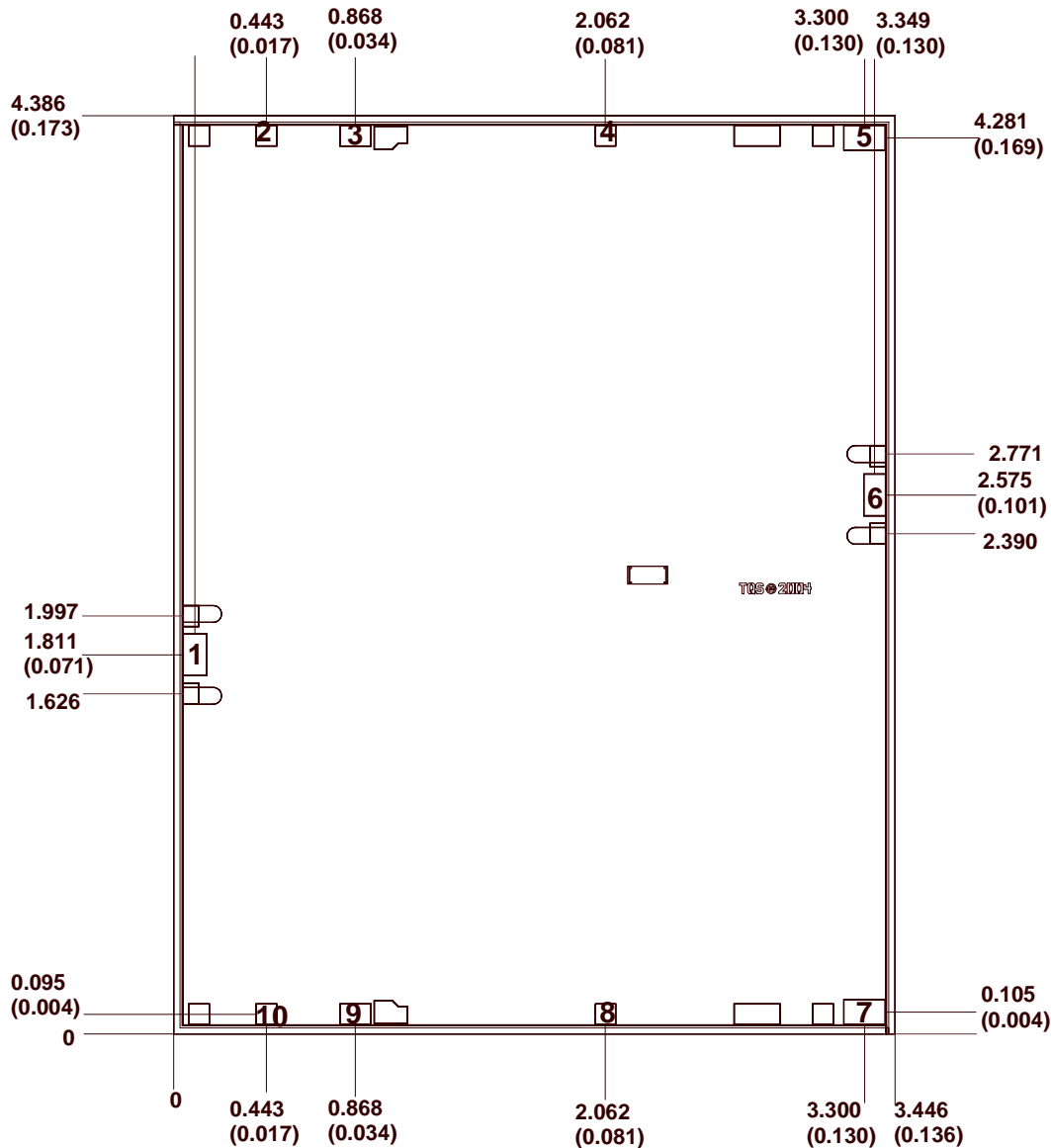
Preliminary Measured Data

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 2\text{ A}$



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Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

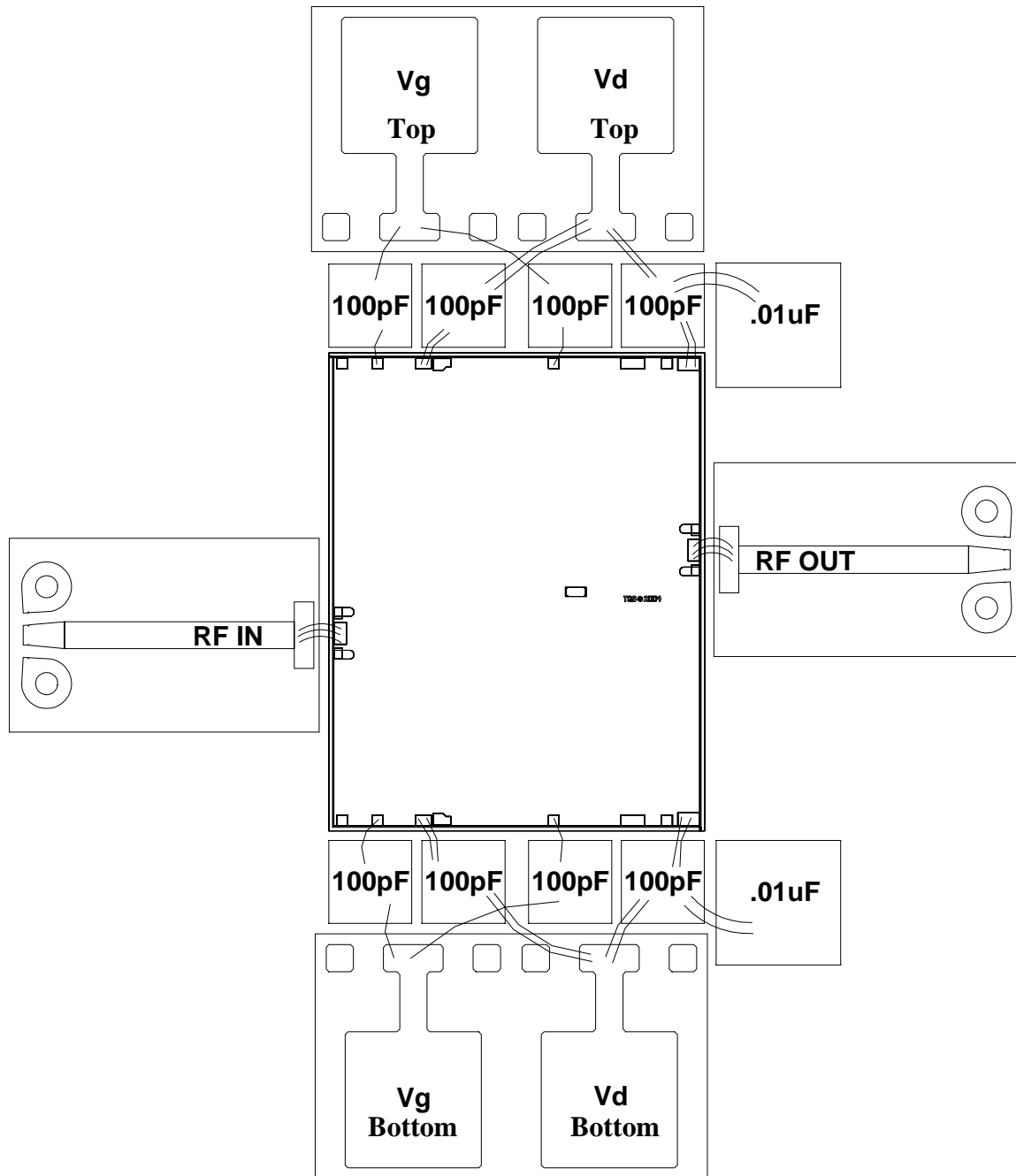
GND is back side of MMIC

Bond pad #1:	(RF In)	0.114 x 0.200 (0.004 x 0.008)
Bond pad #2, #4, #8, #10:	(Vg)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #3, #9:	(Vd)	0.150 x 0.100 (0.006 x 0.004)
Bond pad #5, #7:	(Vd)	0.200 x 0.120 (0.008 x 0.005)
Bond pad #6:	(RF Out)	0.105 x 0.200 (0.004 x 0.008)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Recommended Chip Assembly Diagram

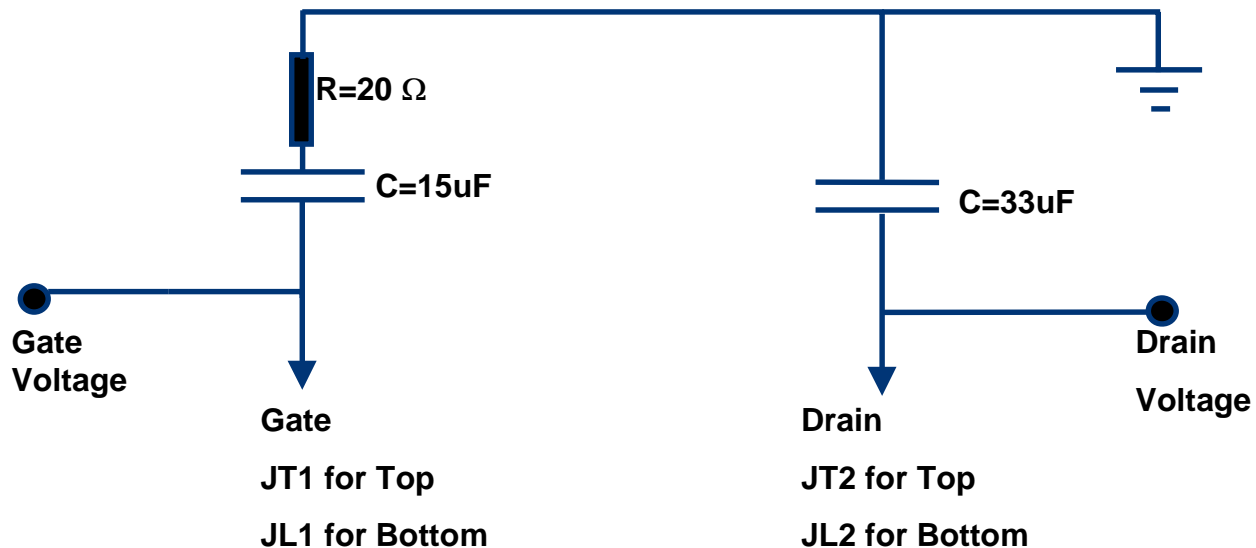


The TFNs at both RF in and RF out are flare TFNs with dimensions of 0.01 x 0.03 in on 0.01 in thick Alumina substrate.

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Recommended Test Setup Diagram



Biasing setup procedures

- (1) Recommend use conductive thermal grease underneath carrier for proper operation. Also use cooling fan to improve heat dissipation.
- (2) Before applying bias, set gate supply voltage to -1.5V and current limit to 4mA on each half of the amplifier, then apply the bias to gate.
- (3) Set drain supply voltage to 1V and current limit to 1.6A on each half of the amplifier, then apply the bias to drain.
- (4) Slowly increase the gate supply voltage and check the drain current, if drain current slowly increases, then increase drain supply voltage slowly to 6V.
- (5) Slowly adjust gate supply voltage to obtain a drain current of 1A quiescent on each half of the amplifier.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300⁰C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200⁰C.

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